Version 02 Mezzanine on the 16MB board

Thoughts and notes:-

CY62167DV30 needs to be connected to a total of 21 address lines to fully decode each of the 2M x 8bit bytes

AS6C3216 needs to be connected to a total of 22 address lines to fully decode each of the 4M x 8bit bytes

Only the AS6C3216 chip uses Pin 10, therefore Pin 10 should be the highest address bit !!

Both the CY62167DV30 and AS6C3216 use Pin 45 (in byte mode) as an address input, this should be the next address below that used on pin10

Taking mezzanine (byte) interleaving (bA0) into account (2 mezzanines)

CY62167DV30 needs buffered addresses bA1 to bA20 to be connected to chip A0 to A19, bA21 should be connected to Pin 45

AS6C3216 needs buffered addresses bA1 to bA20 to be connected to chip A0 to A19, bA21 should be connected to Pin 45 & bA22 should be connected to Pin10

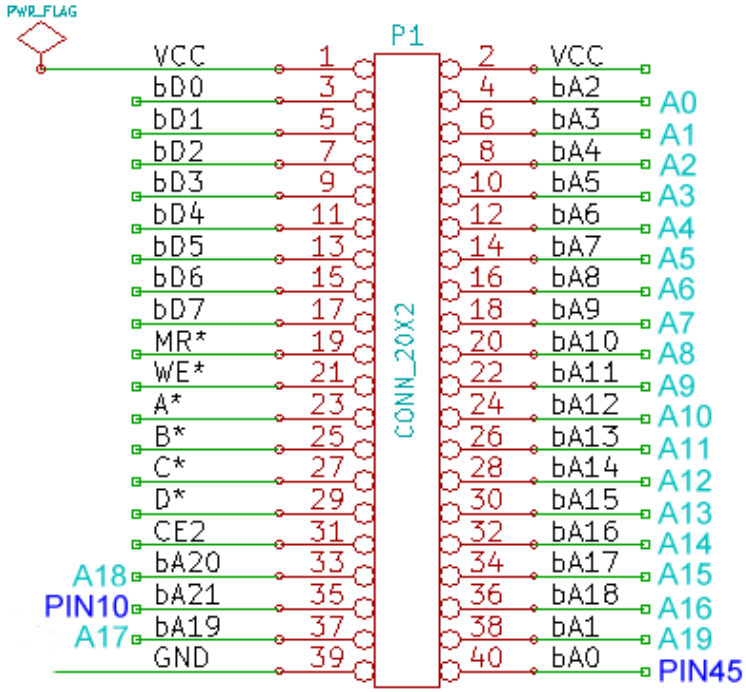
In the case of CY62167DV30 bA22 & bA23 is decoded by U4a to address 4 chips per mezzanine (A*, B*, C* & D*)

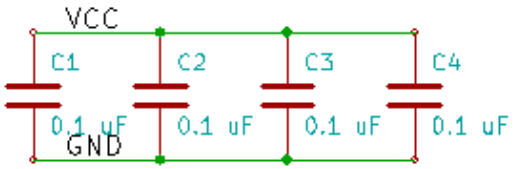
In the case of AS6C3216 only bA23 is decoded by U4a (see previous sent doc for mod details)

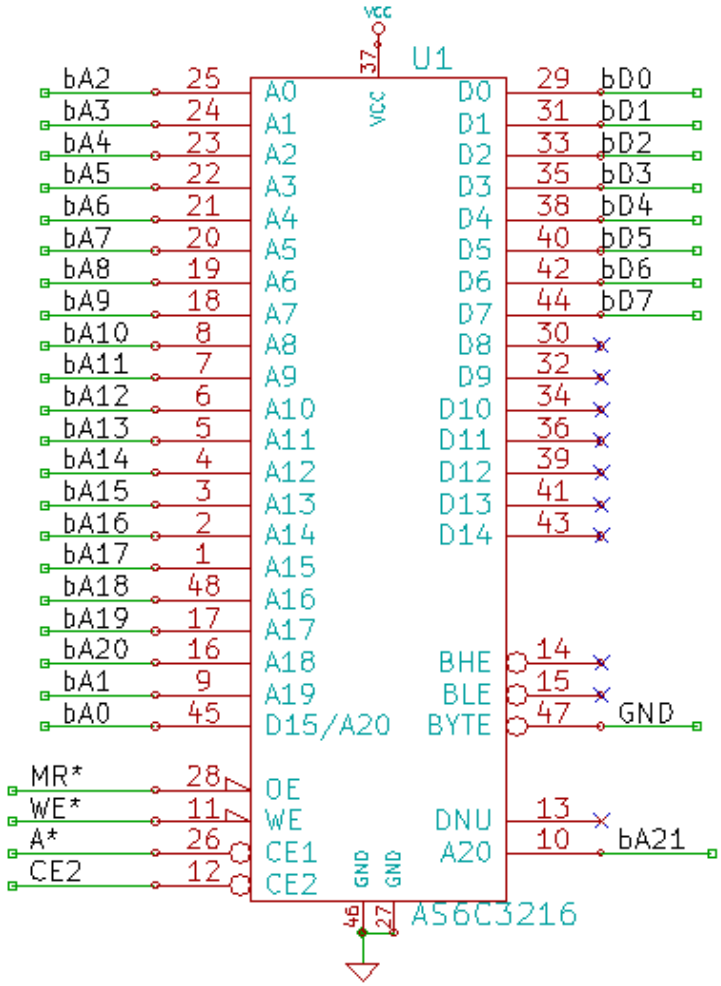
Summary

We only need be concerned that Pin 45 of the SRAM is bA21, and Pin 10 of the SRAM (AS6C..) is bA22

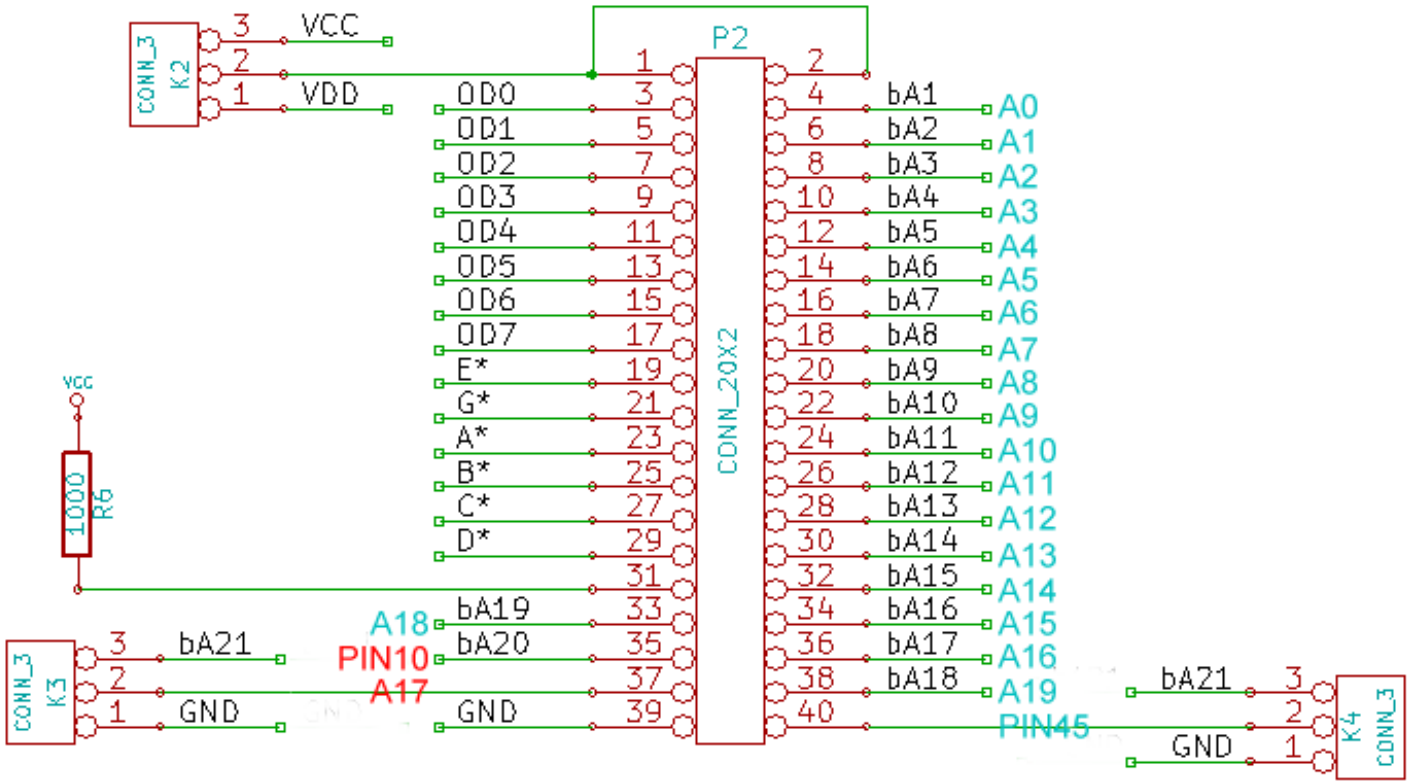
Mezzanine V02 PCB (2nd Mar 2014)







Mezzanine Header on 16MB SRAM Board (23rd Mar 2014)



On the two diagrams above ignore the black ‘net’ names bA...etc, I have superimposed onto the connector pins the actual SRAM pinout to see how things line up with a V02 mezzanine (2nd March 2014) on the 16MB SRAM Board (23rd March 2014).

Comparing the two images we see that addresses A0 to A16 line up perfectly then A17 to A19 things go wobbly, the order of these pins doesnt matter as long as they stay within the range bA18 – bA20 as mentioned in the notes above. Our only problem chip address line is A17 (Pin 37 of the header) this needs to be connected to bA20 to fullfill the above requirements then all will be OK.

We note also that Header Pin 40 which connects to SRAM chip Pin 45 can also be jumpered for bA21 fullfilling the requirement for both SRAM chips.

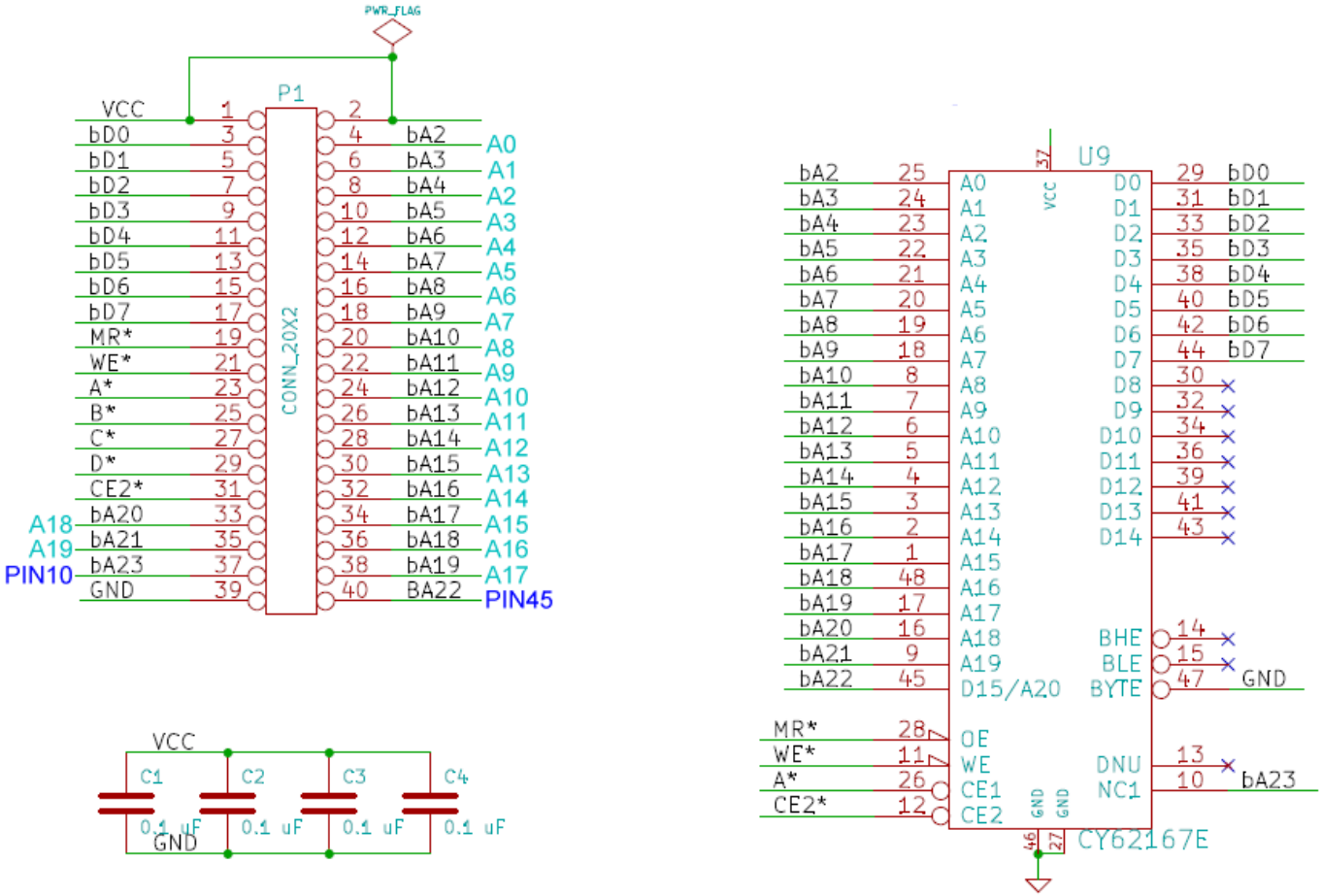
SO... the V02 mezzanine can be patched for the CY62167DV30 by linking mezzanine pins 35 and 37 together as you have already indicated on your website because Pin 10 of the CY62167DV30 is not connected to anything...

BUT... this mezzanine is not usable for the AS6C3216 because by default Mezzanine Pin 35 which connects to Pin 10 of the SRAM chip which in the case of the AS6C3216 needs to be bA22 !!

Possible fix :- transpose pins 35 and 37 on the mezzanine PCB so that SRAM Pin 10 comes out on Header Pin 37, then jumper block K3 pin 3 could be changed to bA22 making is easier to use both types of memory on the same mezzanine.

Version 6 Mezzanine on the 16MB board

Mezzanine V6 PCB (30th March 2014)



Now lets look at the version 6 mezzanine:-

Again ignoring the black ‘net’ names bA...etc, I have superimposed onto the mezzanine connector pins the actual SRAM pinout to see how the V6 mezzanine (2nd March 2014) lines up with the 16MB SRAM Board (23rd March 2014).

Comparing the image above with the SRAM board header picture above we can see that the chip address lines A0 to A16 line up perfectly, A17 now follows on in sequence connected to bA18 on the SRAM board, A18 and A19 also follow in sequence connected to SRAM board bA19 and bA20 respectively.

Pin 45 of the SRAM chip connects to Pin 40 of the header making it jumperable on K4 to bA21 Perfect !

Pin 10 of the SRAM chip connects to Pin 37 of the header permitting wire patching to bA22 on the SRAM board for the AS6C3216 chip.
(K3 Pin 3 needs to be changed to bA22 in a future version of the SRAM board)

SO... the version 6 mezzanine will work with the CY62167DV30 on the 16MB SRAM V1 board without modification.

The version 6 mezzanine can also be used to take the AS6C3216 SRAM chips with a little patching on the 16MB SRAM V1 board (see notes below) to reduce chip count and save money.

Modifiying the 16MB SRAM V01 Board to take the AS6C3216

First let it be said that this modification is for those users who are confident in their abilities to carry out the necessary patches and also have a full understanding of the theory behind the modification and all the notes listed in this document (above), It is not intended for the novice builder. These memory chips are expensive and mistakes can be very costly, It is advise to print out this document and study it in detail before you decide to invest in this modification.

A later version/release of the 16MB SRAM board may include these modifications but this will likely not be for some time to come.

Theory of operation :-

In its normal un-modified form the 16MB SRAM board has been designed to take 8 x 2MB SRAM chips (CY62167DV30) laid out on 2 mezzanine panels which plug onto the SRAM main board, 4 chips per mezzanine.

Looking at the mezzanine header pins 23,25,27,29 we notice 4 chip select lines A*, B*, C* & D*, each one selecting one of the 4 SRAM chips mounted on the mezzanine. These lines are also commoned between the two mezzanine panels to enable 2 chips to be addressed at one time for 16 bit operation. For 8 bit operation the read/write signals on Pins 19 & 21 are gated/steered through the 8/16 bit data selection circuit (U9, U12, U13 etc...) which facilitates the interleaving of the two mezzanines, one mezzanine for odd addresses the other for even..

Therefore if we wish to use a higher capacity SRAM chip such as the AS6C3216 to reduce chip count and hence cost, we need to mount two chips on each mezzanine to maintain functionality for 8 and 16 bit mode. If all 4 chip were mounted on one mezzanine, in 16 bit mode we would only have half of a 16 bit word, and in 8 bit mode we would have only odd OR even address locations.

Truth Table For U4A

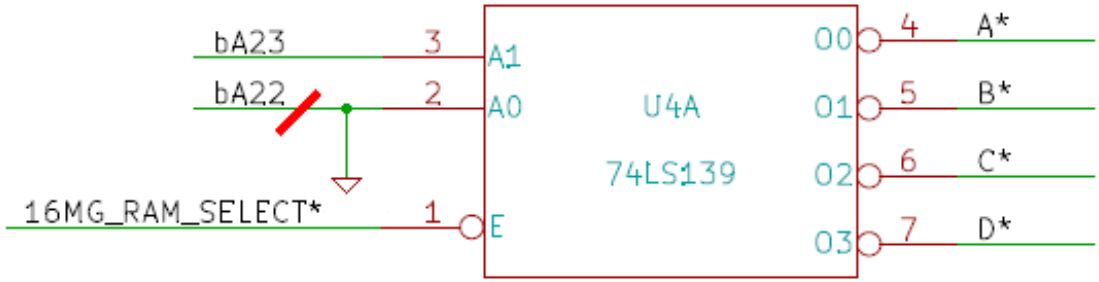
A1 (bA23)	A0 (bA22)	Active Output	
0	0	O0	A*
0	1	O1	B*
1	0	O2	C*
1	1	O3	D*

Looking at the truth table above for U4A we can see how the chip select lines (A*, B*, C* & D*) are generated from address lines bA23 and bA22 for the 4 SRAM chips on each mezzanine. In order to use the higher capacity AS6C2316 4MB SRAM chip we need to redirect bA22 onto Pin 37 of the mezzanine header and facilitate a way of producing just two chip select outputs.

Taking note of the dotted red line which diagramatically shows the address range area of the two AS6C2316 SRAM chips, we can see that bA23 can be used to generate the 2 chip select lines we require if we suppress the changes on A0 (Pin 2 of U4A) by strapping it to ground.

The blue boxed areas in column A0 can just be thought of as 2 x 2MB pages inside the 4MB SRAM chip. We achieve the desired result by cutting a trace (bA22) leading to Pin 2 of U4A and pulling Pin 2 to ground, our two chip select lines will then be A* and C* (because A0 is tied low) and this determines the locations on the mezzanine panels where we need to solder our SRAM chips.

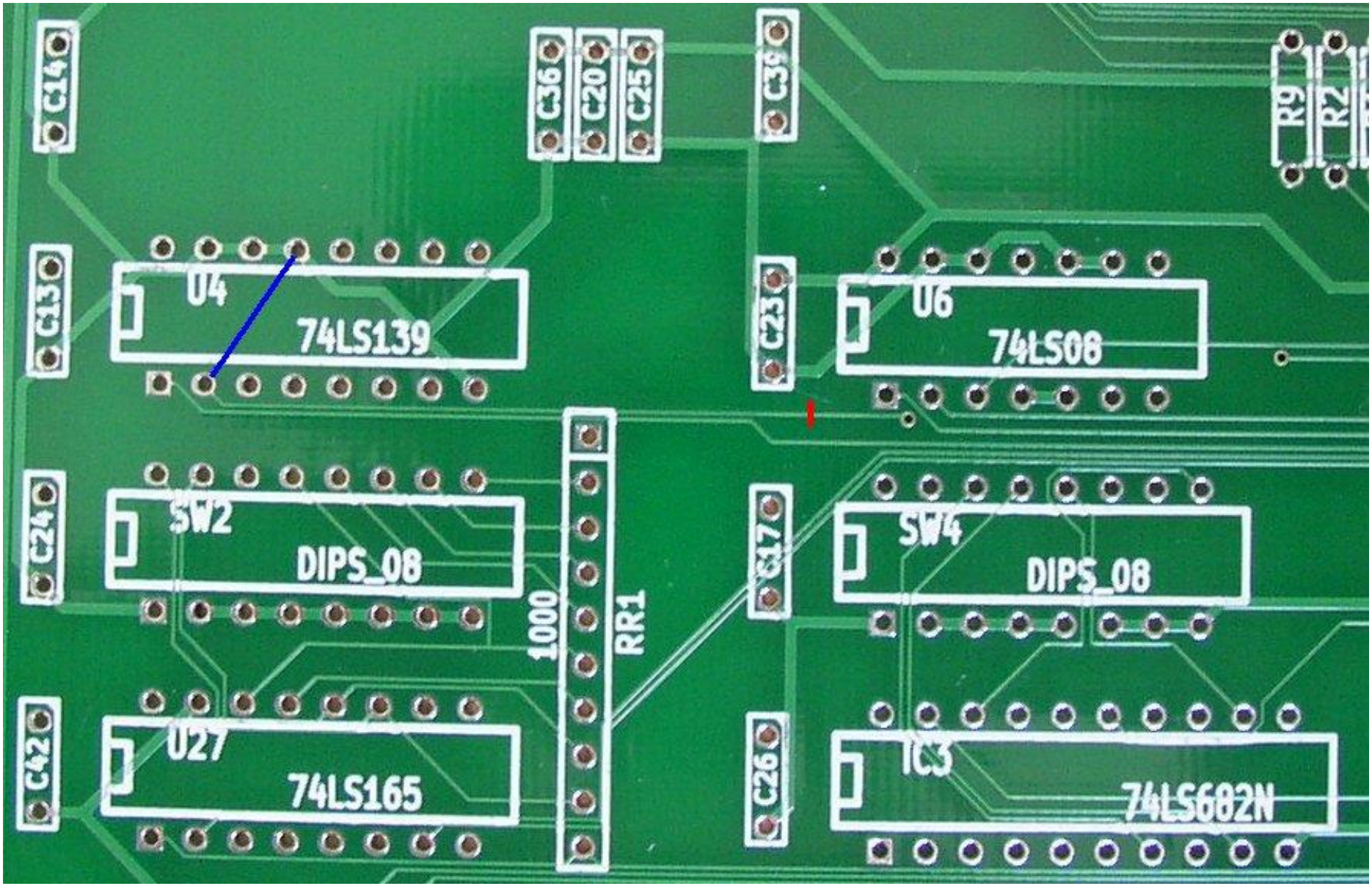
U4A SRAM Chip Select Decoder



The diagram above shows the changes to U4A discussed above in schematic form, the red line indicates a cut in the signal trace bA22, pin 2 is then tied to GND.

The picture below shows the best location to cut the signal trace bA22 that feeds pin 2 of U4, the red line indicates component side, and the blue line indicates where to add the wire link to ground pin 2 of U4, this will need to be mounted on the copper (non- component side)

Note:- Pins 8, 13, 14, & 15 are all ground, diagram shows pin 13 for reasons of clarity.

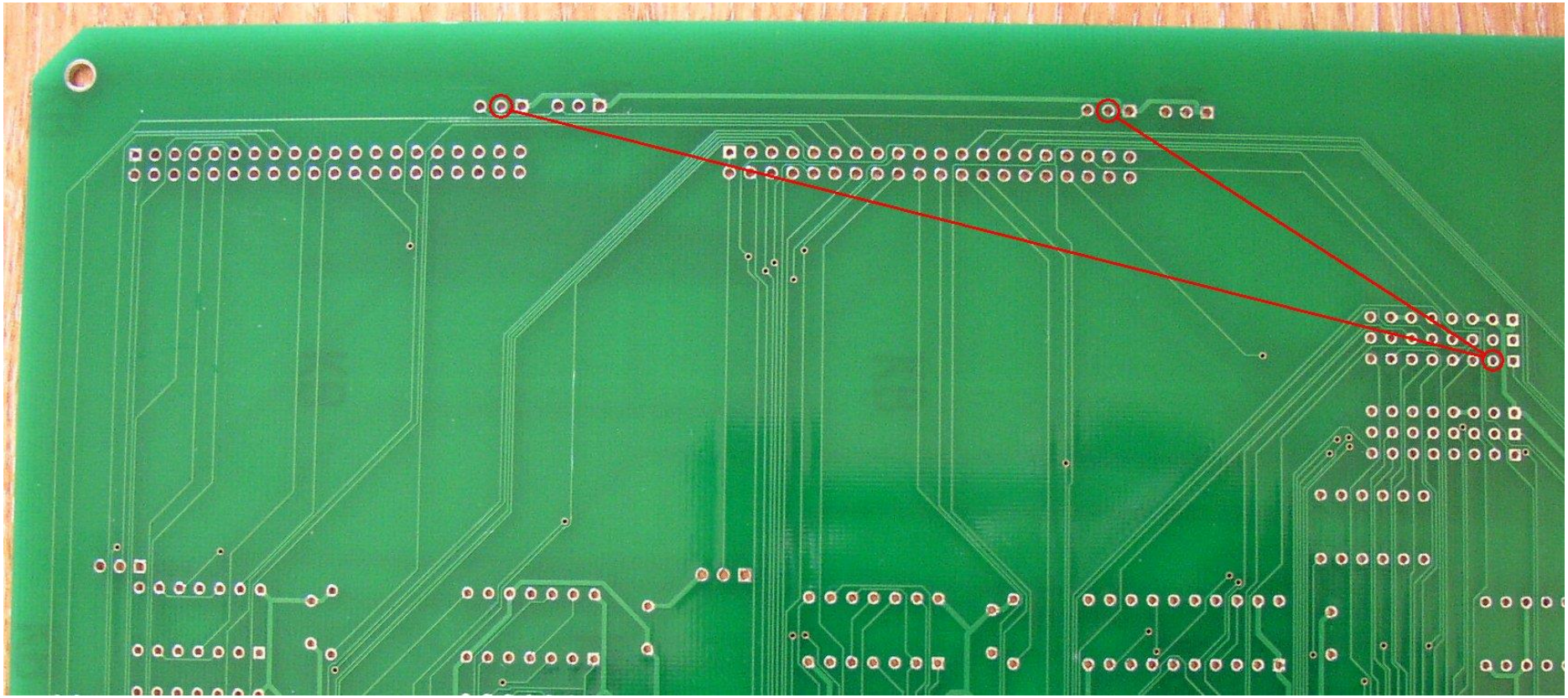

C14
C36
C20
C25
C30
R9
R2
U4
74LS139
C13
C23
U6
74LS08
C24
SW2
DIPS_08
1000
RR1
C17
SW4
DIPS_08
C42
U27
74LS165
C26
IC3
74LS682N

The remaining two wire links pick up address line bA22 and connect it to Pin 37 on each mezzanine header via jumpers K3 and K6

Solder one wire link from Pin 2 of jumper P49 to Pin 2 of jumper K3

Solder the other link from Pin 2 of jumper P49 to Pin 2 of jumper K6

This completes the wire link patches.

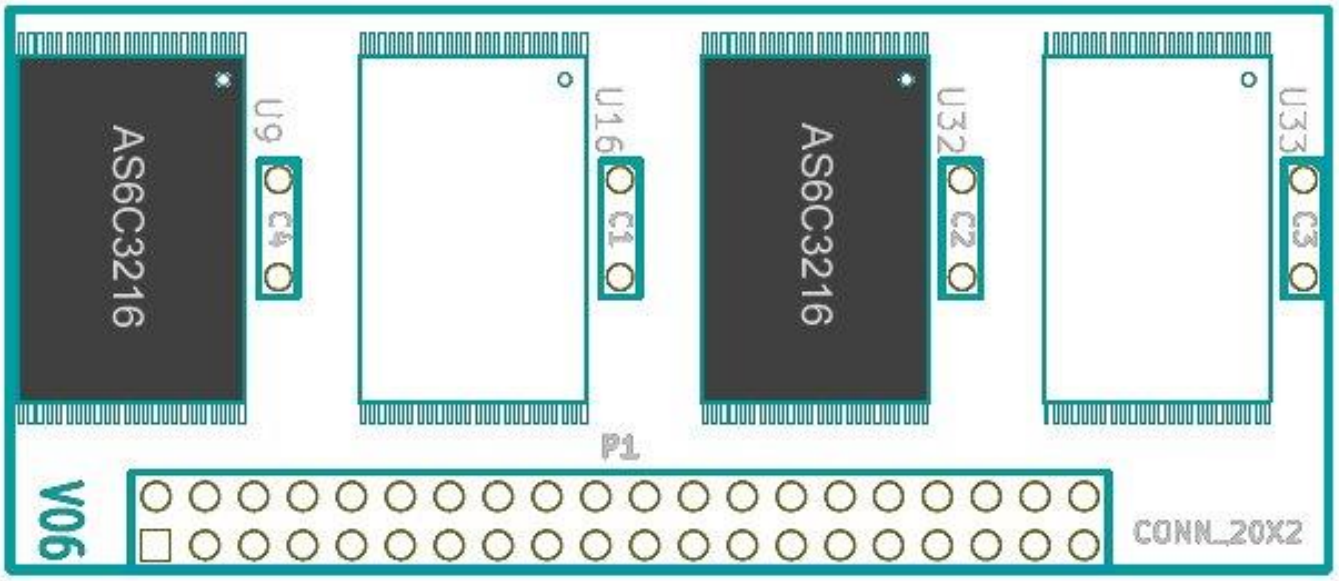


Finally solder 2 x AS6C3216 SRAM chips into locations U9 and U32 on each of the two mezzanines (4 chips in total)

as shown in to picture below taking care to observe the correct orientation of Pin 1, mistakes are costly at $22 approx per chip.

Take care to ensure that the 16MB SRAM board is jumpered for 3.3v memory devices (K2, 1-2 and K5, 1-2)

Then fit both mezzanines to the 16MB SRAM board and check other board configuration jumpers and set as necessary.



You should now have a full 16MB RAM address range at just over half the cost of using the Cypress CY62167DV30

The AS6C3216 is available from Digikey part number 1450-1026-ND at approx $21.00 each